LISTING OF THE CLAIMS:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1: (Currently Amended) An apparatus which comprises:

a multi-core processor and

at least one test control mechanism, including at least one test access port controller (TAPC) and a plurality of distributed data and control registers;

wherein said at least one test access port controller (TAPC) and at least one of said plurality of distributed data and control registers are coupled via an Integrated Test Bus (ITB)

said multi-core processor and said test control mechanism having a configuration so as to allow testing of said multi-core processor.

2: (original) The apparatus of claim 1, wherein said multi-core processor comprises at least two processor cores and at least one circuit comprising non-processor core logic.

3: (original) The apparatus of claim 2, wherein said multi-core processor and said test control mechanism having a configuration so as to allow testing of at least two processor cores of said multi-core processor.

4: (Previously Presented) The apparatus of claim 2, wherein said plurality of distributed data and control registers are located both within said at least two processor cores and within said at least one circuit comprising non-core logic.

5: (original) The apparatus of claim 4, wherein said at least one test control mechanism is substantially compliant with the IEEE 1149.1 specification.

6: (original) The apparatus of claim 4, wherein said at least one test access port controller (TAPC) is located within said at least two processor cores.

7: (Cancelled) .

8: (original) The apparatus of claim 4, wherein said distributed test control mechanism is controllable, at least in part, by one of said at least one test access port controller (TAPC).

9: (Previously Presented) The apparatus of claim 8, wherein which one of said at least one test access port controllers (TAPCs) controls said distributed test control mechanism is dynamically selectable during operation.

10: (original) The apparatus of claim 2, wherein at least one of the said at least two processor cores comprises one test access port (TAP) which includes one test access port controller (TAPC), and a plurality of distributed data and control registers.

11: (original) The apparatus of claim 10, wherein said test control mechanism and said at least two processor cores are coupled so as to provide multiple coupling arrangements, said multiple coupling arrangements being dynamically selectable during operation.

12: (original) The apparatus of claim 11, wherein said multiple coupling arrangements are selected from a group consisting essentially of coupling said test access ports substantially in series, coupling said test access ports substantially in parallel and coupling said test access ports for substantially independent operation.

13: (original) The apparatus of claim 10, wherein said at least one test control mechanism is arranged to allow at least one of said at least two processor cores' said one test access port (TAP) to be externally visible from said multi-core processor.

14: (original) The apparatus of claim 13, wherein said at least one test control mechanism is arranged to allow only one of said at least two processor cores' said one test access port (TAP) to be externally visible from said multi-core processor.

15: (original) The apparatus of claim 13, wherein said at least one test control mechanism is arranged to allow the selection of which at least one of said at least two processor cores' said one test access port (TAP) is externally visible from said multi-core processor to occur dynamically.

16: (original) The apparatus of claim 10, wherein said at least one test control mechanism is coupled to produce during operation an error signal if the output signals of said at least two processor cores' said one test access port (TAP) are not substantially equivalent.

17: (original) The apparatus of claim 2, wherein said at least one test control mechanism, said at least one processor core and said at least one circuit comprising non-processor core logic are

further coupled so as to allow testing of said at least one circuit comprising non-processor core logic.

18: (Currently Amended) A system which comprises:

a computing platform, including:

a memory to store instructions;

a multi-core processor to process instructions which includes:

a plurality of processor cores;

at least one circuit comprising non-processor core logic and

a test control mechanism, including at least one test access port controller (TAPC) and a plurality of distributed data and control registers,

wherein said at least one test access port controller (TAPC) and at least one of said a plurality of distributed data and control registers are coupled via an Integrated Test Bus (ITB);

said multi-core processor and said test control mechanism having a configuration so as to allow testing of said plurality of processor cores.

19: (Previously Presented) The system of claim 18, wherein said multi-core processor and said test control mechanism are capable of allowing testing of said at least one circuit comprising non-processor core logic.

20: (Previously Presented) The system of claim 18, wherein said plurality of distributed data and control registers are located both within said plurality of processor cores and within said at least one circuit comprising non-core logic.

21: (original) The system of claim 20, wherein said at least one test control mechanism is substantially compliant with the IEEE 1149.1 specification.

22: (original) The system of claim 20, wherein said at least one test access port controller (TAPC) is located within said plurality of two processor cores.

23: (Cancelled) .

24: (original) The system of claim 20, wherein said distributed test control mechanism is controlled, at least in part, by one of said at least one test access port controller (TAPC).

25: (Previously Presented) The system of claim 24, wherein which one of said at least one test access port controllers (TAPCs) controls said distributed test control mechanism is be dynamically selected during operation.

26: (original) The system of claim 18, wherein each of the said at least two processor cores comprises one test access port (TAP) which includes one test access port controller (TAPC), and a plurality of distributed data and control registers.

27: (original) The system of claim 26, wherein said test control mechanism and said at least two processor cores are coupled so as to provide multiple coupling arrangements, said multiple coupling arrangements being dynamically selected during operation.

28: (original) The system of claim 27, wherein said multiple coupling configurations are selected from a group consisting essentially of coupling said test access ports substantially in series, coupling said test access ports substantially in parallel, and coupling said test access ports for substantially independent operation.

29: (original) The system of claim 26, wherein said test control mechanism is coupled to produce, during operation, a signal that indicates whether the output signals of said at least two processor cores' said one test access port (TAP) are equivalent or substantially equivalent.

30-37: (Cancelled).